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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/819,990	03/29/2001	Isao Minematsu	57454-060	3710

7590 06/26/2006

EXAMINER	

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ART UNIT	PAPER NUMBER

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Please find below and/or attached an Office communication concerning this application or proceeding.

Notification of Non-Compliant Appeal Brief (37 CFR 41.37)	Application No.	Applicant(s)	
	09/819,990	MINEMATSU, ISAO	
	Examiner	Art Unit	
	Daniel Pan	2183	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The Appeal Brief filed on *14 April 2006* is defective for failure to comply with one or more provisions of 37 CFR 41.37.

To avoid dismissal of the appeal, applicant must file anamended brief or other appropriate correction (see MPEP 1205.03) within **ONE MONTH or THIRTY DAYS** from the mailing date of this Notification, whichever is longer. **EXTENSIONS OF THIS TIME PERIOD MAY BE GRANTED UNDER 37 CFR 1.136.**

1. ☐ The brief does not contain the items required under 37 CFR 41.37(c), or the items are not under the proper heading or in the proper order.

2. ☐ The brief does not contain a statement of the status of all claims, (e.g., rejected, allowed, withdrawn, objected to, canceled), or does not identify the appealed claims (37 CFR 41.37(c)(1)(iii)).

3. ☐ At least one amendment has been filed subsequent to the final rejection, and the brief does not contain a statement of the status of each such amendment (37 CFR 41.37(c)(1)(iv)).

4. ☒ (a) The brief does not contain a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by page and line number and to the drawings, if any, by reference characters; and/or (b) the brief fails to: (1) identify, for each independent claim involved in the appeal and for each dependent claim argued separately, every means plus function and step plus function under 35 U.S.C. 112, sixth paragraph, and/or (2) set forth the structure, material, or acts described in the specification as corresponding to each claimed function with reference to the specification by page and line number, and to the drawings, if any, by reference characters (37 CFR 41.37(c)(1)(v)).

5. ☐ The brief does not contain a concise statement of each ground of rejection presented for review (37 CFR 41.37(c)(1)(vi))

6. ☐ The brief does not present an argument under a separate heading for each ground of rejection on appeal (37 CFR 41.37(c)(1)(vii)).

7. ☐ The brief does not contain a correct copy of the appealed claims as an appendix thereto (37 CFR 41.37(c)(1)(viii)).

8. ☐ The brief does not contain copies of the evidence submitted under 37 CFR 1.130, 1.131, or 1.132 or of any other evidence entered by the examiner **and relied upon by appellant in the appeal**, along with a statement setting forth where in the record that evidence was entered by the examiner, as an appendix thereto (37 CFR 41.37(c)(1)(ix)).

9. ☐ The brief does not contain copies of the decisions rendered by a court or the Board in the proceeding identified in the Related Appeals and Interferences section of the brief as an appendix thereto (37 CFR 41.37(c)(1)(x)).

10. ☒ Other (including any explanation in support of the above items):

See Continuation Sheet.

Continuation of 10. Other (including any explanation in support of the above items): This is a response to the Supplemental Appeal Brief on April 14, 2006. As to the Summary of Claimed Subject Matter set forth in page 2 of the Brief, although appellent cited the figs.1A,B, 2 and Pages 7-10, in the specifcation regarding the microprocessor and the components of memory, decoder, PC, ALU and the TR0-TR3, R0-R3 registers, no teaching of the claimed single instruction code can be found. Appellant also cited Figs.4-11 and Pages 10-16 as having the teaching of a single instruction having a single operation code fetched by the PCU 40. However, upon a further review, the fig.4-7 show more than just a single instruction. For example, the fig.7 shows three instructions for a store (ST TR0, X:AR3, MV TR, AR0, and ST TR, X:AR3). Another example is in Fig.9, it shows a single macro instruction PUSH with a plurality of sub-instructions (see PUSH in Fig.9B has at least first instruction x_memory[sp]=tr0 and a second instruction tr0=ra). Regarding the fig.10, it shows a push (1), but it is not the transfer between registers nor transfer between registers and memory. The push R0 (2) involves at least two instructions as set forth in Fig.9 B. Therefore, it is not a single instruction code with one operation as claimed. It appears that the appellant's a single instruction code is actually a macro instruction as shown in the push ra in Fig.9B. The evidence also shows that appellent is directed a macro instruction (see fig.14, Page 17, lines 25-32). A macro instruction is a single instruction as taught by priot art of record (see ADD macro instruction in col.6, lines 28-37 in Boggs et al. 5,687,338 as cited by examiner on record). Appellant argued that Bogg's ADD instruction, for example, is not a single instruction with a single operation code. The position has been held by examiner that Boggs also taught a single instruction code (ADD eax, mem) having a single operation code (ADD). See Bogg's col.6, lines 28-37, see also the citation in page 3 of last Office action on 08/22/05. Nevertheless, appellant's push ra instruction is composed of at least two instruction codes and having more than one operations : x_memory[sp] = tr0 and tr0=ra (see fig.9B). Therefore, appellant is suggested to provide a clear teaching of "a single instruction code having a single operation code" in the specification in order to clarify the issue. The question is what is a single instruction code having a single operation when appellant's teaching shows a single macro instruction composed of at least two subinstruction codes having more than just one operation ? For the above reasons, appellant is herein requested to show the "single instruction code having a single operation code" described in the specification by particular page number and line number in order to simply the issue. The concise explanation of the subject matter in the independent claim 1 by referring to pages and line numbers has not been met. In the Supplemental Appeal Brief, appellant only referred back the page and figure numbers, but no line number was included. Therefore, the isssue of what appellant's "single instruction" really is has not been clear. Furthemore, appellant did not identify for each dependent claim argued separately described in the specifcation by page number and line number. Therefore, 37 C.F. R. 41.37 has not been met by the Supplemental Appeal Brief on April, 14, 2006 .

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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